What is claimed is:

Sub A' 1. A frame-relay frame transmission circuit wherein, when a received frame-relay frame is written in a memory, said frame is written from an address shifted from the top of a frame buffer.

2. A frame-relay frame transmission circuit according to claim 1, wherein the shift size is determined for each connection.

3. A frame-relay frame transmission circuit for reassembling a frame-relay frame into an Asynchronous Transfer Mode (ATM) cell comprising:

a processor for determining a shift size for each connection, said shift size by which said frame is to be shifted from the top address of a frame buffer;

a frame receiver for receiving said frame through said connection;

a memory for storing said received frame in a frame buffer from an address shifted from the top of a frame buffer by said shift size; and

a segmentation and reassembling device for reassembling said frame into said ATM cell.

4. A frame-relay frame transmission circuit according to claim 3, wherein said processor writes the set of a data link connection identifier (DLCI) and said shift size into a connection table, and retrieves said shift size in said connection table using said DLCI as a key.

5. A frame-relay frame transmission circuit according to claim 3, wherein said frame received by said frame receiver is transmitted to said memory through direct memory access.

6. A method for reassembling a frame-relay frame into an Asynchronous Transfer Mode (ATM) cell comprising the steps of:

determining a shift size for each connection by which said frame is to be shifted from the top address of a frame buffer in a memory;

receiving said frame and writing said frame from an address shifted from the top address of said frame buffer by said shift size; and

reassembling said frame into an ATM cell.

7. A method according to claim 6, further comprising the steps of:

writing a set of a data link connection identifier (DLCI) and said shift size into a connection table; and

retrieving said shift size in said connection table using said DLCI as a key.

8. A method according to claim 6, wherein said received frame is transmitted to said memory through direct memory access.

9. A computer readable medium containing program instructions for reassembling a frame-relay frame into an Asynchronous Transfer Mode (ATM) cell, the program instructions including instructions for performing the steps comprising:

determining a shift size for each connection by which said frame is to be shifted

from the top address of a frame buffer in a memory;

receiving said frame and writing said frame from an address shifted from the top address of said frame buffer by said shift size; and

reassembling said frame into an ATM cell.

10. A computer readable medium according to claim 9, wherein said program instructions include instructions for:

writing a set of a data link connection identifier (DLCI) and said shift size into a connection table; and

retrieving said shift size in said connection table using said DLCI as a key.

11. A computer readable medium according to claim 9, wherein said received frame is transmitted to said memory through direct memory access.